Appendix W6.7.2
Digital Implementation of Example 6.15

EXAMPLE W6.1 *Lead Compensation for a DC Motor*

As an example of designing a lead compensator, let us repeat the design of compensation for the DC motor with the transfer function

$$G(s) = \frac{1}{s(s+1)},$$

that was carried out in Section 5.4.1. This also represents the model of a satellite-tracking antenna (see Fig. 3.60). This time we wish to obtain a steady-state error of less than 0.1 for a unit-ramp input. Furthermore, we desire an overshoot of $M_p < 25\%$.

1. Determine the lead compensation satisfying the specifications.
2. Determine the digital version of the compensation with $T_s = 0.05$ sec.
3. Compare the step and ramp responses of both implementations.

Solution.

1. The steady-state error is given by

$$e_{ss} = \lim_{s \to 0} s \left[\frac{D_c}{1 + KD_c(s)G(s)} \right] R(s), \qquad \text{(W6.1)}$$

where $R(s) = 1/s^2$ for a unit ramp, so Eq. (W6.1) reduces to

$$e_{ss} = \lim_{s \to 0} \left\{ \frac{1}{s + KD_c(s)[1/(s+1)]} \right\} = \frac{1}{KD_c(0)}.$$

Therefore, we find that $KD_c(0)$, which is the steady-state gain of the compensation, cannot be less than 10 ($K_v \geq 10$) if it is to meet the error criterion, so we pick $K = 10$. To relate the overshoot requirement to PM, Fig. 6.37 shows that a PM of 45° should suffice. The frequency response of $KG(s)$ in Fig. W6.1 shows that the PM $= 20°$ if no phase lead is added by compensation. If it were possible to simply add phase without affecting the magnitude, we would need an additional phase of only 25° at the $KG(s)$ crossover frequency of $\omega = 3$ rad/sec. However, maintaining the same low-frequency gain and adding a compensator zero would

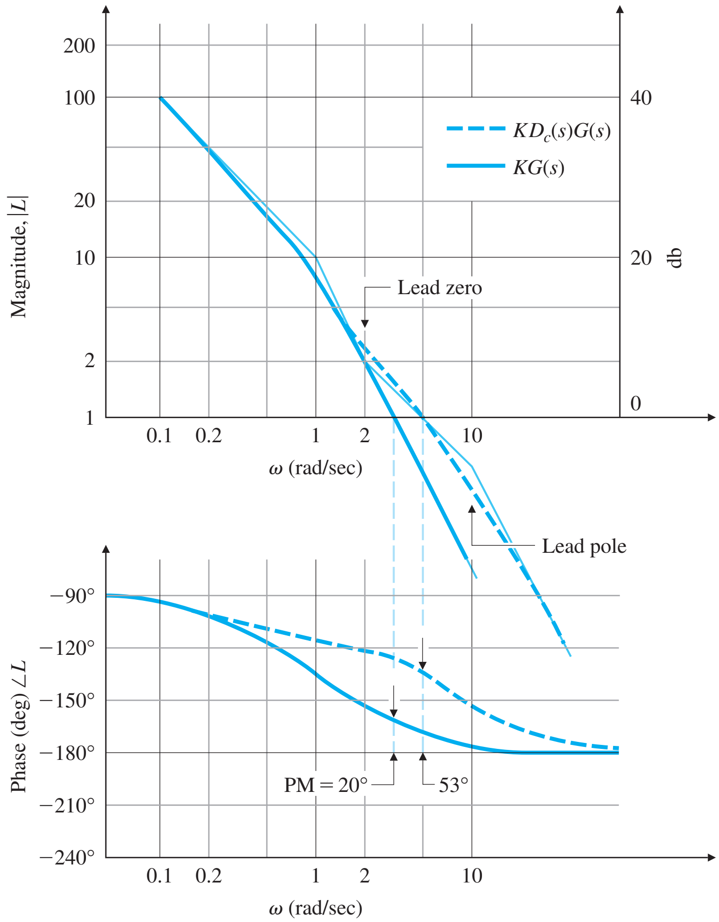

Figure W6.1
Frequency response for lead-compensation design

increase the crossover frequency; hence, more than a 25° phase contribution will be required from the lead compensation. To be safe, we will design the lead compensator so that it supplies a maximum phase lead of 40°. Fig. 6.53 shows $1/\alpha = 5$ will accomplish that goal. We will derive the greatest benefit from the compensation if the maximum phase lead from the compensator occurs at the crossover frequency. With some trial and error, we determine that placing the zero at $\omega = 2$ rad/sec and the pole at $\omega = 10$ rad/sec causes the maximum phase lead to be at the crossover frequency. The compensation, therefore, is

$$KD_c(s) = 10\frac{s/2+1}{s/10+1}.$$

The frequency-response characteristics of $L(s) = KD_c(s)G(s)$ in Fig. W6.1 can be seen to yield a PM of 53°, which satisfies the design goals.

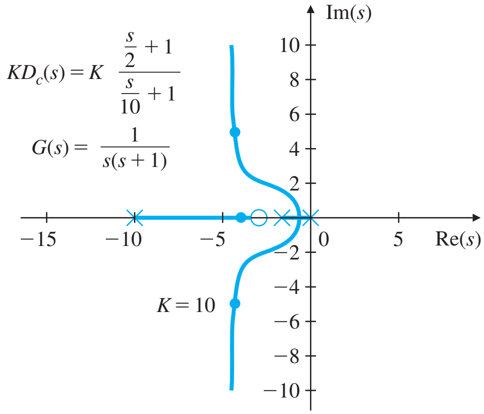

Figure W6.2
Root locus for lead-compensation design

The root locus for this design, originally given as Fig. 5.24, is repeated here as Fig. W6.2, with the root locations marked for $K = 10$. The locus is not needed for the frequency-response design procedure; it is presented here only for comparison with the root locus design method presented in Chapter 5. The entire process can be expedited by the use of Matlab's sisotool design tool, which simultaneously provides the root locus and the Bode plot through an interactive GUI interface. For this example, the Matlab statements

```
G=tf(1,[1 1 0]);
Dc=tf(10*[1/2 1],[1/10 1]);
sisotool(G,Dc)
```

will provide the plots as shown in Fig. W6.3. It also can be used to generate the Nyquist and time-response plots if desired.

2. To find the discrete equivalent of $D_c(s)$, we use the trapezoidal rule given by Eq. (W4.31). That is,

$$D_d(z) = \frac{\frac{2}{T_s}\frac{z-1}{z+1}/2+1}{\frac{2}{T_s}\frac{z-1}{z+1}/10+1}, \tag{W6.2}$$

which, with $T_s = 0.05$ sec, reduces to

$$D_d(z) = \frac{4.2z-3.8}{z-0.6}. \tag{W6.3}$$

This same result can be obtained by the Matlab statements

```
sysDc = tf([0.5 1],[0.1 1]);
sysDd = c2d(sysDc, 0.05, 'tustin').
```

Because

$$\frac{U(z)}{E(z)} = KD_d(z), \tag{W6.4}$$

the discrete control equation that results is

$$u(k+1) = 0.6u(k) + 10(4.2e(k+1) - 3.8e(k)). \tag{W6.5}$$

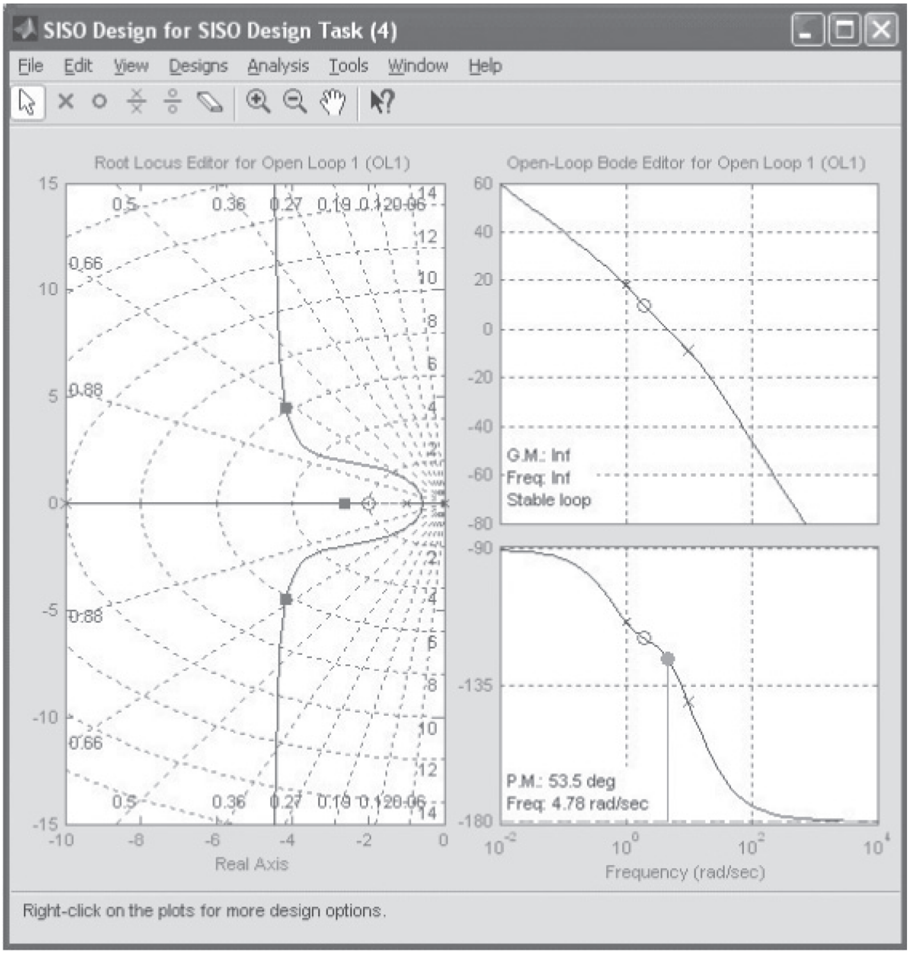

Figure W6.3

SISOTOOL graphical interface for Example W6.1

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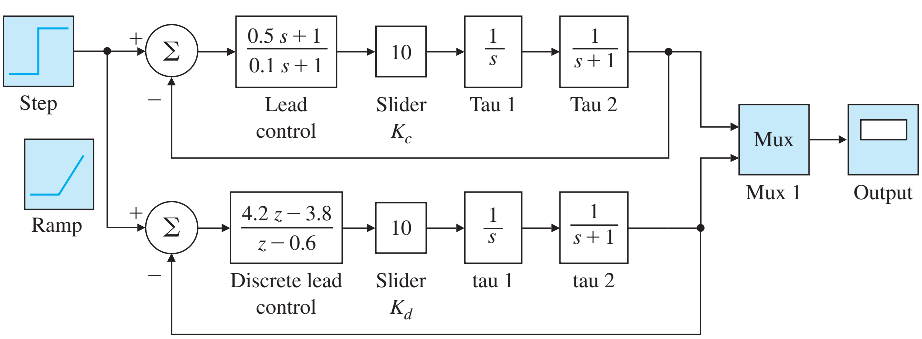

Figure W6.4

Simulink block diagram for transient response of lead-compensation design

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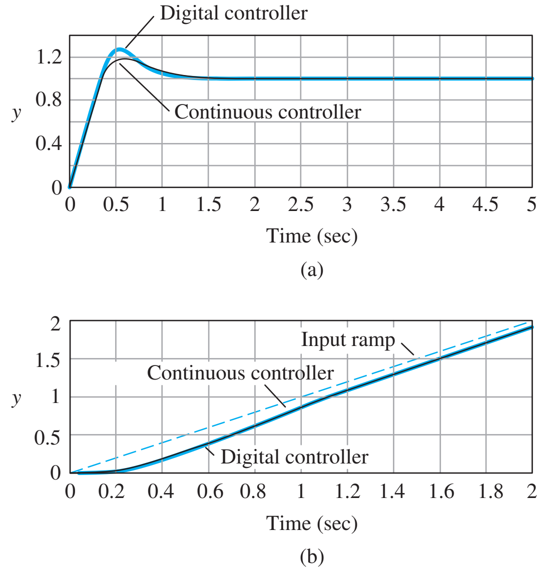

Figure W6.5
Lead-compensation design: (a) step response; (b) ramp response

3. The Simulink block diagram of the continuous and discrete versions of $D_c(s)$ controlling the DC motor is shown in Fig. W6.4. The step responses of the two controllers are plotted together in Fig. W6.5a and are reasonably close to one another; however, the discrete controller does exhibit slightly increased overshoot, as is often the case. Both overshoots are less than 25%, and thus meet the specifications. The ramp responses of the two controllers, shown in Fig. W6.5b, are essentially identical, and both meet the 0.1 specified error.