Control of Sputter Process for Improved Run-to-run Repeatability

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1. Introduction

Radio frequency (RF) diode sputtering deposition is a widely used process for depositing GMR thin films for multilayers, spin valves, spin-dependent tunneling (SDT) devices, etc [1]. However, the thin films thus produced often show signification variation in GMR properties from wafer to wafer. As described in the earlier chapter, a multiscale model based on the primary physical phenomena - gas flow, plasma discharge, sputtering and atom transport has been developed to explore the sputter deposition process. Simulations with this model were used to determine the process parameters to which the deposition characteristics have the maximum sensitivity. Experiments were performed to determine the relative importance of these parameters. Based on the results, a controller was designed to regulate the time-integrated target bias voltage. Implementation of the controller reduced wafer-to-wafer variation of GMR properties by over 50%. Additionally, application of control to SDT wafers also led to improvement and optimization of the process.

2. Measurement of Variation in Process Conditions

GMR multilayer wafer processing consists of depositing a stack of as many as sixteen layers of metals in a specific order, including three conducting layers of copper-silver-gold (CuAgAu, 16.5 Å), six layers of ferromagnetic cobalt-iron (CoFe, 15 Å), four layers of nickel-cobalt-iron (NiCoFe, 20 Å and 40 Å). The three properties of these wafers that are used to measure performance are the GMR percentage, saturation magnetic field strength (h_{sat}), and the sheet resistance (ρ). Among these three, h_{sat} is the property most sensitive to wafer level variations such as deposition thickness of the various layers (especially that of the critical copper layer). As shown in Figure 1, h_{sat} data show considerable variation from wafer-to-wafer, even when the nominal CuAgAg thickness is constant. As discussed in the Chapter 9, it is seen that h_{sat} can go out of acceptable range with relatively small changes in power, chamber temperature, pressure, and electrode spacing.

The sputter chamber was instrumented in order to monitor the four process parameters (power, pressure, temperature, and spacing) over several deposition cycles. The chamber's existing position and pressure sensors were used for measuring electrode spacing and background gas pressure, respectively. An RTD was used to measure the chamber wall temperature. A relatively simple dynamic thermal model of the chamber showed that conduction dominated heat transfer. The gas inside the chamber was essentially at the wall temperature and responded to temperature changes very quickly. As a result, the chamber wall temperature is a good indicator of the Ar temperature. The target bias voltage is the DC component of the voltage between the sputter target and ground. This voltage varies directly with the input RF power, and can be measured with fewer modifications to the set-up than RF power itself. Hence, the target bias voltage was measured using a voltage divider circuit instead of measuring RF power. All the measurements were made using SC's Solutions data acquisition and control hardware/software product, RT-iCon™ with 16-bit A/D conversion.

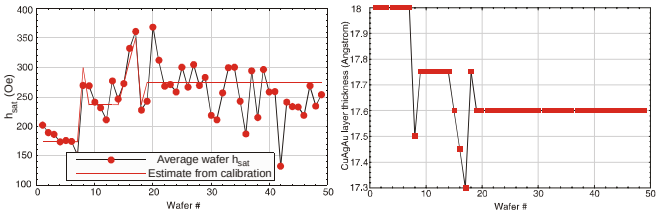

Figure 1: Run-to-run variation in data from NVE.

Figure 2 shows the results of the monitoring the processing of several wafers over two days. The saturation field strengths, h_{sat}, are plotted against the measured process parameters. It is seen that only the target bias voltage correlates significantly with wafer h_{sat}. The chamber pressure is controlled to within 0.1% at the point of measurement. There is a small variation in the electrode spacing of 0.4 mm (1%) from wafer-to-wafer due to the precision limitations of the wafer pallet motion controller. There is also a small variation in the chamber temperature of 2°C over the two days. Since the cooling water temperature, measured before entering the chamber,

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showed little change over the two days, the wall temperature variation was probably caused by fluctuations in the room temperature. Figure 2 shows that reducing the power variations will have a larger effect on reducing GMR property variations than better control of electrode spacing or chamber temperature. Improvements to spacing and temperature control would also be more complicated and expensive to implement involving substantial modifications to the chamber, especially in a production environment.

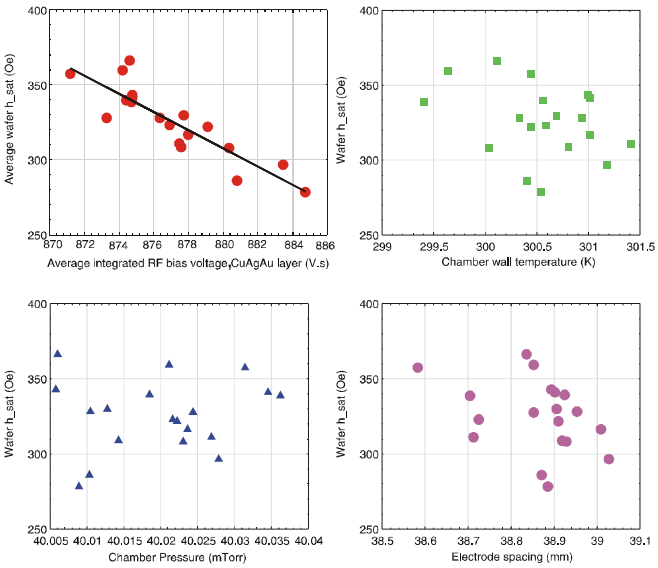

Figure 2: Correlation between process variables and wafer property.

The primary cause of the variation in the integrated target bias voltage (and thus, the net RF power input to the plasma) is apparent when the data collected at 200 Hz is plotted in Figure 3. The plots show the recorded voltages for three CuAgAu layers for a multilayer wafers. At an approximate deposition rate of 200 Å/min, the 16.5 Å layer takes 5 s for deposition. Figure 3 has a magnified view of the initial part of the deposition cycle when most of the voltage variation (>1% of the mean voltage) occurs. These voltage fluctuations correspond to plasma transients that occur at the onset of the plasma, and are irreproducible.

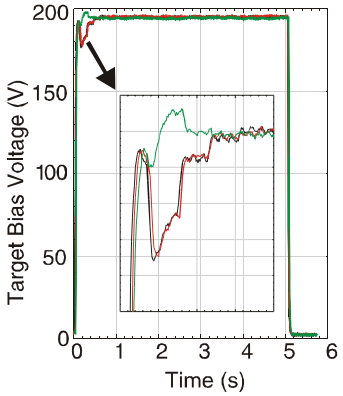

Figure 3: Effect of plasma transients on target bias voltage from run-to-run.

In order to achieve film thickness repeatability from layer-to-layer, the key is to ensure that the *total* number of atomic layers deposited remain unchanged from layer to layer and from wafer to wafer. However, it is not necessary that the deposition *rates* be identical. While the target bias voltage at any instant is a measure of the instantaneous RF power input to the plasma, the time-integrated bias voltage is a measure of the total number of argon ions striking the target[1], which determines the number of neutrals sputtered from the target. The sputtered atom count, in turn, determines the number of atoms deposited on the wafer, and hence, the film thickness. Consequently, repeatability in film thickness may be improved by regulating the integrated bias voltage which effectively meters the number of atoms deposited.

Integrated Bias Voltage Control

A controller was designed to compensate for RF bias voltage fluctuations by adjusting the time the plasma was on so as to regulate the time-integrated voltage (for all layers of the same material deposited). A schematic representation of the controller is shown in Figure 4. The controller computes the integral of the voltage in real-time, and shuts off RF power when the reference value of this integral is reached. The reference value is obtained during calibration (or 'sweep' runs) when the CuAgAu layer thickness is varied until GMR % is maximized with the sheet resistance and h_{sat} is within the range of acceptance. The integrated voltage controller was implmented on SC's RT-iCon™, a real-time, hardware/software platform for implementing embedded model-based feedback control technology. The x86-based hardware platform has a small footprint, and the computing power necessary for implementing complex, high performance and non-linear multi-input-multi-output (MIMO) controllers. The hardware includes necessary I/O capabilities for data acquisition and control, and for communicating with other remote clients *via* standard ethernet-based TCP/IP networking. As shown in Figure 4, one such client is the supervisory computer from which RT-iCon™ receives reference integrated voltages, wafer numbers, operation modes, etc. Other clients may communicate with RT-iCon™ during processing to perform other tasks, e.g., downloading data files for analysis.

[1] This assumption is valid for relatively small changes in the average bias voltage, i.e., negligible changes in the deposition rate.

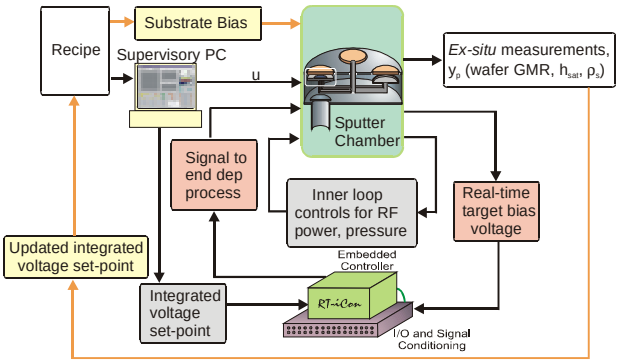

Figure 4: Sputter deposition control strategy.

The controller was designed to operate in either of the following two modes. For calibration runs, RT-iCon™ was operated in sweep mode with deposition time periods for each layer as input. The deposition proceess for each layer was stopped at the end of the specified time, and the integrated bias voltage was reported as output. In control mode, the integrated voltage control for each of the layers was specified as input and deposition ended when the integrated voltage reached this recipe value.

The variation in the integrated bias voltage without control was found to be in the range of 1%-1.5% on an average for all the layers. Use of the feedback controller reduced this variaiton ot less than 0.1% on average. The effect of this regulation on the GMR properties was found to be very significant. Figure 5 shows that as a result of voltage control, the standard deviation in the average GMR % from wafer-to-wafer was reduced by 65% (down to 0.16% from 0.42%). The standard deviation in the sheet resistance was reduced by 52% (from 0.15 Ω down to 0.07 Ω). The saturation magnetic field strength, h_{sat}, showed similar improvements in repeatability with clustering around two mean values. As seen in Figure 5, there is a step jump in h_{sat} after the nineteenth wafer was processed. The standard deviation of these two groups (wafers # 1-19, and wafers # 20-27) showed an average decrease of 46% compared to the group without voltage control.

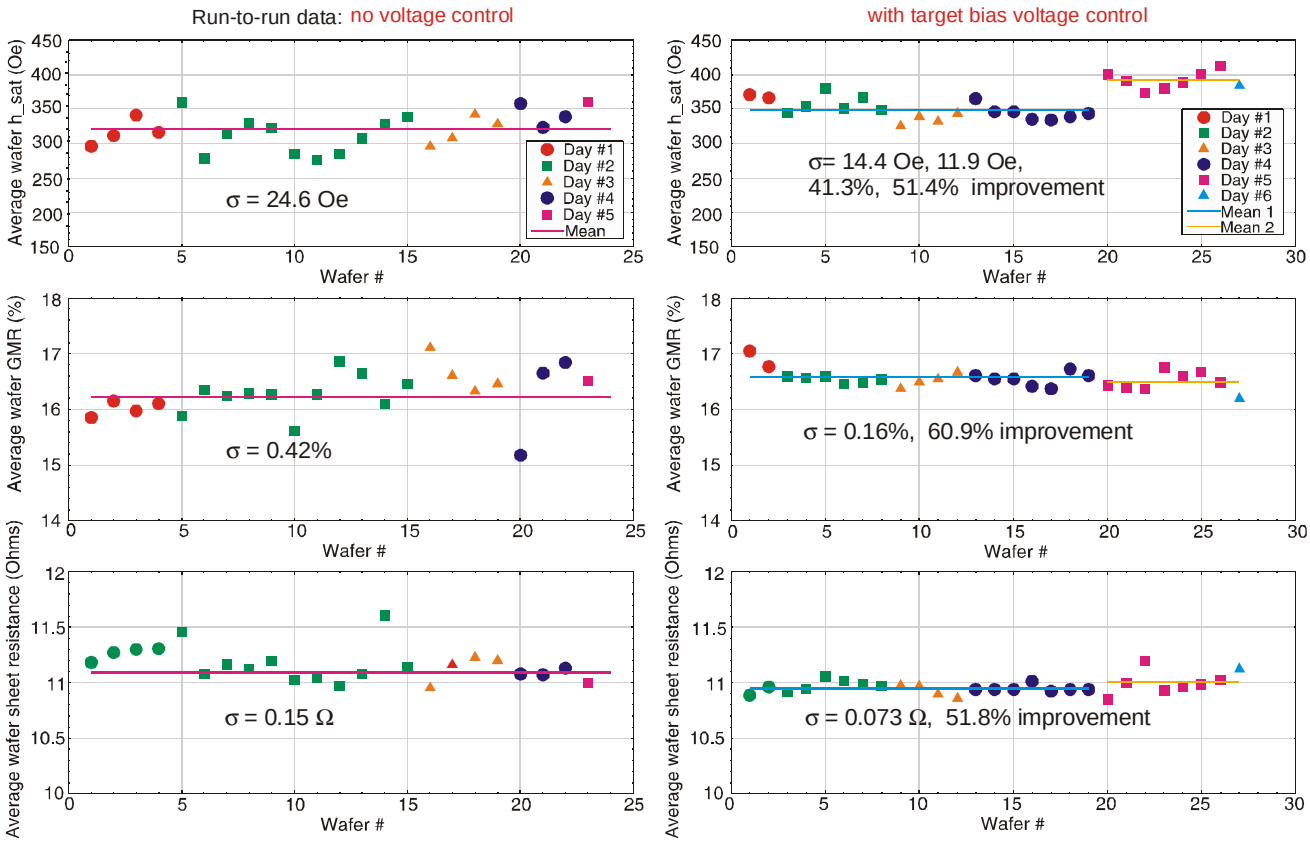

Figure 5: Effect of integrated bias voltage control on GMR multilayers. The left column shows GMR properties (h_{sat}, GMR% and sheet resistance) without control for wafers processed over a period of five days. The column on the right shows the same properties for wafers processed with voltage control. The percentage improvements are significant.

Figure 6 shows the bias voltage, averaged over the deposition period and over the three CuAuAg layers for each wafer, for the set of wafers deposited under voltage control[2]. It is seen that there is a step decrease in the voltage by about 1% at wafer #19, the same point in the batch where h_{sat} showed a step increase in Figure 5. While the feedback controller can compensate for disturbances due to random plasma transients, it cannot compensate for more substantial changes in the process conditions that may result in biases being introduced. These changes are reflected in the step change in the bias voltage that may alter the plasma and the deposition rate significantly. Such changes may occur for many reasons in a manufacturing environment, e.g., when maintenance work was performed on the chamber in the time between the processing of wafers #19 and #20.

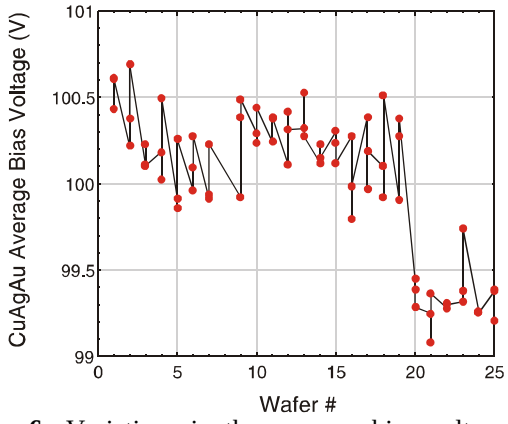

Figure 6: Variations in the *average* bias voltage from wafer to wafer, shown as a percentage of the mean over all the wafers in the set.

A process bias as described above is addressed using the outer loop in Figure 4 that adjusts the integrated voltage set-point using the calibration data, an example of which is shown in Figure 7. The effect of the increased bias voltage on h_{sat} can be offset by depositing a slightly thicker (by 0.25 Å) CuAgAu layer for the next wafer without going out of the acceptable range for GMR and sheet resistance. It is noted that the calibration curves in Figure 7 shift along the x-axis (film thickness) from set to set because of accuracy limitations in measuring the deposition rate which is determined by depositing a thick layer of CuAgAu (about 2000 Å) in a fixed time period. The layer thickness is measured using profilometry to obtain the deposition rate. To deposit films of varying thickness during sweep runs, the corresponding deposition time period is varied accordingly. Uncertainties in the measured deposition rate result in uncertainties in the specified film thickness, and the calibration curve shifts horizontally. However, the slope of the calibration curve is not affected by deposition rate variations but by variations in process parameters that alter key atomic-scale features such as intermixing between atoms of different elements and roughness at the interfaces of various layers are changed. One such parameter could be the wafer temperature that would affect atomic diffusivities.

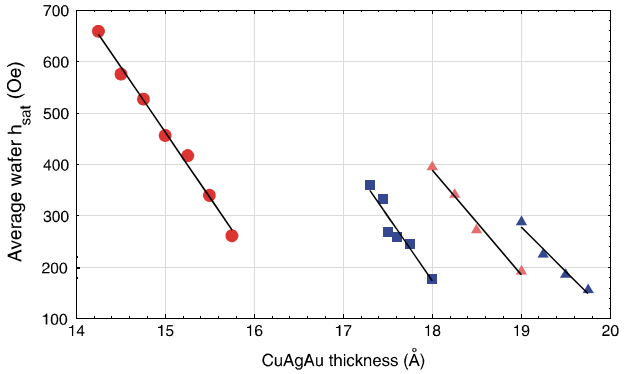

Figure 7: Four sets of calibration data for selecting optimal copper layer `thickness'.

7. SDT Wafers

The controller was used for processing spin dependent tunneling (SDT) wafers that involve depositing permalloy (125 Å), aluminum (12 Å), CoFe (50 Å), and IrMn (100 Å) layers, including the oxidation of very thin aluminum layer lasting 2.6 s. Like the multilayer wafers, SDT wafers showed significant wafer-to-wafer variations in the key properties, *viz.*, the GMR %, sheet resistance, and the Resistance-Area Product (RAP).

Figure 8 shows the results of using voltage control for SDT wafers. At first glance, there appears to be no improvement in repeatability, with the GMR % showing an almost steady decrease as the wafer batch was processed. A closer look at the data collected during the controlled runs, on a layer-by-layer basis, revealed that the bias voltage did not change significantly for four out of the five processes. However, a large change (>6% range over the batch) in bias voltage was observed during CoFe deposition following oxidation (columns 5), indicating a disturbance that affected the plasma. It was concluded that the disturbance was caused by the presence of residual oxygen in the chamber left over from the previous aluminum oxidation process. The recommended solution was to 'burn' the CoFe target for a longer period following oxidation in order to purge the system of the residual oxygen. The source of the problem would not been so easily uncovered without the feedback control in operation.

[2] Note that it is not the integrated bias voltage. For convenient comparison, the voltages are plotted as percent of the average of all the wafers in the set.

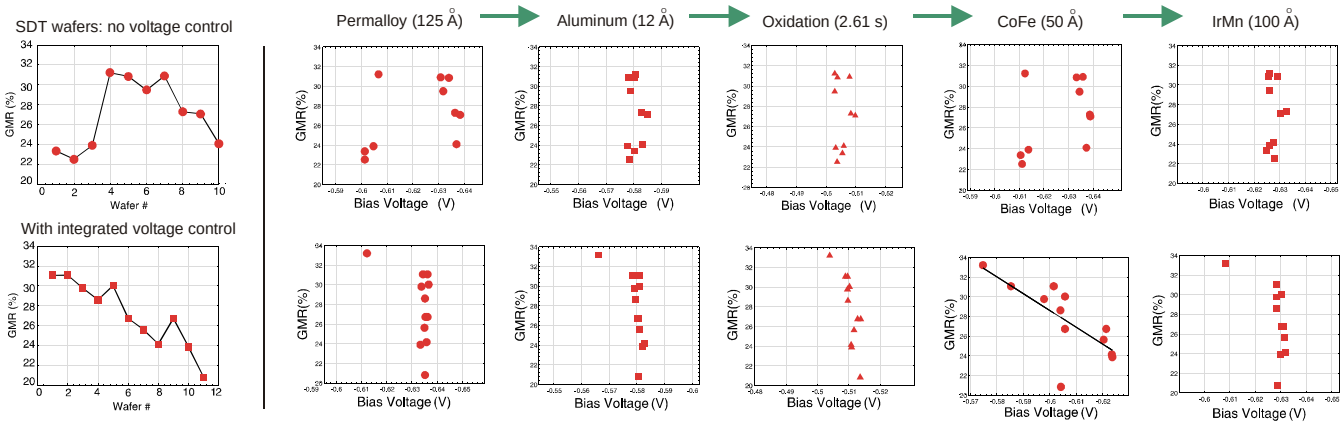

Figure 8: Results with voltage control of deposition for SDT devices.

It is very important for SDT devices that the aluminum oxidation be optimized, i.e., presence of both non-oxidized aluminum and any oxidization of the underlying permalloy layer must be minimized over the wafer surface [2]. In this optimized situation, the GMR % will be maximized with the RAP restricted to within the acceptable range. To this end, experiments were performed with a range of integrated bias voltages for oxidation while keeping the integrated voltages constant for the other steps thus varying the extent of oxidation. Figure 9, with the GMR % plotted against RAP, shows how the optimal integrated voltage for oxidation for maximum GMR is determined. If the RAP corresponding to the maximum GMR is too high (note logarithmic scale), then the curve itself may be translated to the left by depositing a thinner layer of aluminum, and *vice-versa* if the RAP is too low [2].

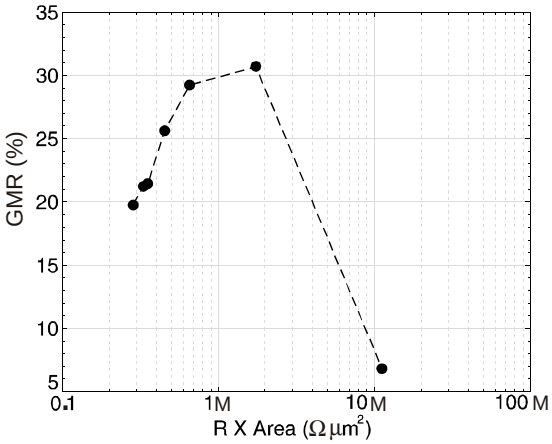

Figure 9: Dependence of GMR on RAP (resistance area product) for SDT wafers.

8. Conclusion

Several experiments were performed on NVE's sputter chamber to determine the relative importance of the process parameters in introducing wafer-to-wafer variability in GMR properties. The experiments were guided by the process model sensitivities (see Chapter 9). The RF power was found to be reasonably well correlated to the saturation magnetic field strength, while the other three parameters (gas temperature and pressure, and electrode spacing) showed poor correlation. A feedback control scheme that regulated the time-integrated target bias voltage was designed and implemented on a hard real-time embedded computer capable of operating at frequencies up to 500 Hz while recording process data. The controller effectively metered the number of sputtered atoms deposited on the wafer, and thus controlled the layer thickness. The control hierarchy also included an outer loop for compensating biases introduced by small changes in process conditions. Use of the controller reduced the wafer-to-wafer variability of GMR properties of multilayer wafers by more than half. The application of the RT-iCon™ controller to SDT illustrates two other uses beyond real-time control for better repeatability. These uses are identification of other critical variabilities introduced by the oxidation process, and process optimization facilitated by good control of layer thickness from wafer to wafer.

References

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2. Song, J. Nowak, and M. Covington, 'Proper Oxidation for Spin Dependent Tunneling Junctions', *44th Annual Conference of Magnetism and Magnetic Materials*, November 1999, San Jose.